What Is Claimed Is:

1. A self-aligned method of forming a semiconductor memory array of floating gate memory cells in a semiconductor substrate, each memory cell having a floating gate, a first terminal, a second terminal with a channel region therebetween, and a control gate, the method comprising the steps of:

a) forming a plurality of spaced apart isolation regions on the substrate which are substantially parallel to one another and extend in a first direction, with an active region between each pair of adjacent isolation regions, the active regions each comprising a first layer of insulation material on the semiconductor substrate and a first layer of conductive material on the first layer of insulation material;

b) forming a plurality of spaced apart blocks of insulation material in each of the active regions and over the first layer of conductive material;

c) forming a plurality of spaced apart blocks of conductive material in each of the active regions that are each disposed over and insulated from the substrate and adjacent to one of the blocks of insulation material;

d) forming a protective layer of material over a first portion of each of the blocks of conductive material, wherein a second portion of each of the blocks of conductive material is left uncovered by the layer of protective material;

e) etching away the second portions of the blocks of conductive material to form a substantially vertical sidewall portion on each of the blocks of conductive material;

f) forming a plurality of first terminals in the substrate, wherein in each of the active regions each of the first terminals has a side edge that is aligned to one of the substantially vertical sidewall portions; and

g) forming a plurality of second terminals in the substrate, wherein in each of the active regions each of the second terminals is spaced apart from the first terminals.

2. The method of claim 1, wherein one of the blocks of conductive material in each of the active regions extends across adjacent isolation regions and is electrically connected with blocks of conductive material formed in adjacent active regions.

3. The method of claim 1, further comprising the steps of:

removing the protective layer of material from the blocks of conductive material, and

forming a layer of metalized silicon on the blocks of conductive material.

4. The method of claim 1, wherein the first layer of conductive material is formed with a plurality of sharp edges each extending toward one of the blocks of conductive material.

5. The method of claim 1, wherein the formation of the protective layer includes the steps of:

forming a layer of insulation material over the second portions of the blocks of conductive material; and

forming a spacer of insulation material over at least part of the first portions of the blocks of conductive material.

6. The method of claim 1, wherein each of the first portions of the blocks of conductive material includes a lower portion that is disposed adjacent to and insulated from the first layer of conductive material.

7. The method of claim 6, wherein each of the first portions of the blocks of conductive material includes an upper portion that extends over and is insulated from a portion of the first layer of conductive material.

8. The method of claim 7, wherein each of the first portions of the blocks of conductive material forms a control gate having a notch formed underneath the upper portion.

9. The method of claim 1, further comprising the steps of:

forming a side wall spacer of insulating material along each of the substantially vertical sidewall portions; and

forming a layer of metalized silicon in each of the first terminals immediately adjacent to one of the side wall spacers, wherein each of the layers of metalized silicon is self-aligned to the one of the first terminals by one of the side wall spacers.

10. The method of claim 9, further comprising the step of:

forming a conductive material over each of the first terminals and against the side wall spacer self aligning one of the layers of metalized silicon thereto.

11. The method of claim 1, further comprising the steps of:

forming a side wall spacer of insulating material along each of the substantially vertical sidewall portions such that pairs of the side wall spacers are adjacent to but spaced apart from each other with one of the first terminals substantially therebetween;

forming a layer of metalized silicon in each one of the first terminals between a pair of the side wall spacers corresponding to the one first terminal such that the layer of metalized silicon is self-aligned to the one first terminal by the corresponding pair of side wall spacers;

forming a layer of passivation material over the active regions;

forming contact openings through the passivation material, wherein for each of the contact openings:

the contact opening extends down to and exposes one of the metalized silicon layers,

the contact opening has a lower portion bounded by the corresponding pair of side wall spacers, and

the contact opening has an upper portion that is wider than a spacing between the corresponding pair of side wall spacers; and

filling each of the contact openings with a conductive material.

12. A self-aligned method of forming a semiconductor memory array of floating gate memory cells in a semiconductor substrate, each memory cell having a floating gate, a first terminal, a second terminal with a channel region therebetween, and a control gate, the method comprising the steps of:

a) forming a plurality of spaced apart isolation regions on the substrate which are substantially parallel to one another and extend in a first direction, with an active region between each pair of adjacent isolation regions, the active regions each comprising a first layer of

insulation material on the semiconductor substrate and a first layer of conductive material on the first layer of insulation material;

b) forming a plurality of spaced apart first trenches across the active regions and isolation regions which are substantially parallel to one another and extend in a second direction that is substantially perpendicular to the first direction and exposing the first layer of the conductive material in each of the active regions;

c) forming first side wall spacers of a material on side walls of the first trenches;

d) forming a second side wall spacer of a material on each of the first side wall spacers;

e) forming second trenches in each of the active regions adjacent to the first trenches, wherein the formation of the second trenches includes removing the first side wall spacers;

f) filling each of the second trenches with a second conductive material to form blocks of conductive material;

g) forming a protective layer of material over a first portion of each of the blocks of conductive material, wherein a second portion of each of the blocks of conductive material is left uncovered by the layer of protective material;

h) etching away the second portions of the blocks of conductive material to form a substantially vertical sidewall portion on each of the blocks of conductive material;

i) forming a plurality of first terminals in the substrate, wherein in each of the active regions each of the first terminals has a side edge that is aligned to one of the substantially vertical sidewall portions; and

j) forming a plurality of second terminals in the substrate, wherein in each of the active regions each of the second terminals is spaced apart from the first terminals.

13. The method of claim 12, wherein one of the blocks of conductive material in each of the active regions extends across adjacent isolation regions and is electrically connected with blocks of conductive material formed in adjacent active regions.

14. The method of claim 12, further comprising the steps of:

removing the protective layer of material from the blocks of conductive material, and

forming a layer of metalized silicon on the blocks of conductive material.

15. The method of claim 12, wherein the first layer of conductive material is formed with a plurality of sharp edges each extending toward one of the blocks of conductive material.

16. The method of claim 12, wherein for each of the blocks of conductive material:

the block is insulated from the substrate, and

the block includes a protruding portion, formed by an indentation in the second trench side wall, that is disposed over and insulated from the first layer of conductive material.

17. The method of claim 16, wherein each of the first portions of the blocks of conductive material forms a control gate having a notch underneath the protruding portion.

18. The method of claim 12, wherein a lower portion of each of the first portions of the blocks of conductive material is disposed adjacent to and insulated from the first layer of conductive material.

19. The method of claim 12, wherein the formation of the first trenches comprises the steps of:

forming at least one layer of material over the first layer of conductive material;

selectively etching through the at least one layer of material to form top portions of the first trenches, wherein the first and second spacers are then formed in the first trenches; and

etching between the second side wall spacers in each of the first trenches and through the first layer of conductive material to form bottom portions of the first trenches;

wherein the bottom portions of the first trenches have a smaller width than that of the top portions of the first trenches.

20. The method of claim 12, further comprising the steps of:

forming a third side wall spacer of insulating material along the substantially vertical side wall portion of each of the blocks of conductive material; and

forming a layer of metalized silicon in each of the second terminals immediately adjacent to one of the third side wall spacers, wherein the layer of metalized silicon is self-aligned to the one third side wall spacer.

21. The method of claim 20, further comprising the step of:

forming a conductive material over each of the first terminals and against the third side wall spacer self aligning one of the layers of metalized silicon thereto.

22. The method of claim 12, further comprising the steps of:

forming a third side wall spacer of insulating material along each of the substantially vertical sidewall portions such that pairs of the third side wall spacers are adjacent to but spaced apart from each other with one of the first terminals substantially therebetween;

forming a layer of metalized silicon in each one of the first terminals between a pair of the third side wall spacers corresponding to the one first terminal such that the layer of metalized silicon is self-aligned to the one first terminal by the corresponding pair of third side wall spacers;

forming a layer of passivation material over the active regions;

forming contact openings through the passivation material, wherein for each of the contact openings:

the contact opening extends down to and exposes one of the metalized silicon layers,

the contact opening has a lower portion bounded by the corresponding pair of third side wall spacers, and

the contact opening has an upper portion that is wider than a spacing between the corresponding pair of third side wall spacers; and

filling each of the contact openings with a conductive material.

23. An electrically programmable and erasable memory device comprising:

a substrate of semiconductor material of a first conductivity type;

first and second spaced-apart regions in the substrate of a second conductivity type, with a channel region therebetween;

a first insulation layer disposed over said substrate;

an electrically conductive floating gate disposed over said first insulation layer and extending over a portion of the channel region and over a portion of the first region;

a second insulation layer disposed over and adjacent the floating gate and having a thickness permitting Fowler-Nordheim tunneling of charges therethrough;

an electrically conductive control gate having a first portion disposed adjacent to and insulated from the floating gate and a second portion extending over a portion of the second insulation layer and a portion of the floating gate, the control gate having a substantially vertical sidewall portion; and

an insulation spacer formed adjacent to the substantially vertical sidewall portion of the control gate;

wherein the second region has an edge that is aligned with the substantially vertical sidewall portion.

24. The device of claim 23, further comprising:

a third insulation layer formed over a top surface of the control gate.

25. The device of claim 23, wherein the floating gate includes a sharp edge portion that extends toward the control gate.

26. The device of claim 25, the first and second portions of the control gate form a notch into which the sharp edge portion of the floating gate extends.

27. The device of claim 23, further comprising:

a layer of metalized silicon formed on the second region and aligned to the insulation spacer.

28. An array of electrically programmable and erasable memory devices comprising:

a substrate of semiconductor material of a first conductivity type;

spaced apart isolation regions formed on the substrate which are substantially parallel to one another and extend in a first direction, with an active region between each pair of adjacent isolation regions;

each of the active regions including a column of memory cells extending in the first direction, each of the memory cells including:

first and second spaced-apart regions formed in the substrate having a second conductivity type, with a channel region formed in the substrate therebetween,

a first insulation layer disposed over said substrate including over said channel region,

an electrically conductive floating gate disposed over said first insulation layer and extending over a portion of the channel region and over a portion of the first region, and

a second insulation layer disposed over and adjacent the floating gate and having a thickness permitting Fowler-Nordheim tunneling of charges therethrough; and

a plurality of electrically conductive control gates each extending across the active regions and isolation regions in a second direction substantially perpendicular to the first direction and having a first portion and a second portion, wherein each of the control gates intercepts one of the memory cells in each of the active regions such that the first portion is positioned adjacent to the second insulation layer and the floating gate and the second portion partially extends over the second insulation layer and the floating gate, and wherein each of the control gates has a substantially vertical sidewall portion; and

a plurality of insulation spacers each formed adjacent to one of the substantially vertical sidewall portions of the control gates;

wherein the second region has an edge that is aligned with the substantially vertical sidewall portion.

29. The device of claim 28, further comprising:

a third insulation layer formed over a top surface of each of the control gates.

30. The device of claim 28, wherein each of the floating gates includes a sharp edge portion that extends toward one of the control gates.

31. The device of claim 30, wherein for each of the control gates, the first and second portions form a notch into which the sharp edge portion of the floating gate extends.

32. The device of claim 28, further comprising:

a layer of metalized silicon formed on each of the second regions and aligned to the corresponding insulation spacer.